CLAIMS

What is claimed is:

1. A method for producing a die assembly comprising the steps of:

providing a wafer stack defining a plurality of die assemblies, the wafer stack having a first wafer and a second wafer, a first die assembly of the plurality of die assemblies being formed of at least a portion of the first wafer and at least a portion of the second wafer;

exposing a portion of the first wafer by removing a portion of the second wafer; and

dicing the exposed portion of the first wafer such that the first die assembly is at least partially separated from the wafer stack.

2. The method of claim 1, wherein the first wafer and the second wafer are arranged in an overlying relationship with each other and bonded together to form the wafer stack.

3. The method of claim 1, wherein the first wafer includes a first component, the first component being arranged adjacent to the second wafer, the first component being configured to electrically communicate with a component external to the wafer stack.

4. The method of claim 1, wherein the wafer stack includes a third wafer, the second wafer being arranged at least partially between the first wafer and the third wafer; and

wherein the step of exposing a portion of the first wafer comprises the step of:

exposing a portion of the first wafer by removing a portion of the third wafer and a portion of the second wafer.

5. The method of claim 1, wherein the step of exposing a portion of the first wafer comprises the steps of:

dicing the second wafer to enable detachment of a portion of the second wafer from the wafer stack; and

removing the portion of the second wafer from the wafer stack.

6. The method of claim 1, wherein the step of dicing the exposed portion of the first wafer comprises the step of:

performing a through-cut of the wafer stack to at least partially detach the first die assembly from the wafer stack.

7. The method of claim 3, wherein the second wafer defines a recessed portion, the recessed portion being arranged in an overlying relationship with the first component, the recessed portion being configured to enable a partial through-cut of the second wafer in a vicinity of the recessed portion such that the first component is not damaged during formation of the partial through-cut; and

wherein the step of exposing a portion of the first wafer comprises the step of:

performing a partial through-cut of the second wafer in the vicinity of the recessed portion such that the first component is not damaged by the partial through-cut.

8. The method of claim 4, wherein the step of exposing a portion of the first wafer comprises the steps of:

exposing a portion of the second wafer by removing a portion of the third wafer; and

exposing a portion of the first wafer by removing a portion of the second wafer.

9. The method of claim 5, wherein the step of dicing the second wafer comprises the step of:

performing a first partial through-cut and a second partial through-cut of the wafer stack to at least partially detach of a portion of the second wafer from the wafer stack, the portion of the second wafer to be detached being arranged between the first partial through-cut and the second partial through-cut.

10. A die assembly formed by the method of claim 1.

11. A wafer stack defining a plurality of die assemblies, said wafer stack comprising:

a first wafer including a first component; and

a second wafer arranged in an overlying relationship with said first wafer, said second wafer being bonded to said first wafer, said first component being arranged adjacent to said second wafer, said second wafer defining a recessed portion, said recessed portion being arranged in an overlying relationship with said first component, said recessed portion being configured to enable a partial through-cut of said second wafer in a vicinity of said recessed portion such that said first component is not damaged during formation of the partial through-cut;

wherein a first die assembly of the plurality of die assemblies is defined by at least a portion of said first wafer and at least a portion of said second wafer.

12. The wafer stack of claim 11, further comprising:

a third wafer, said second wafer being arranged at least partially between said first wafer and said third wafer.

13. The wafer stack of claim 11, wherein said first component is configured to enable communication of said first die assembly with a component external to said first die assembly.

14. The wafer stack of claim 12, wherein said second wafer includes a second component, and wherein said third wafer defines a recessed portion, said recessed portion of said third wafer being arranged in an overlying relationship with said second component, said recessed portion of said third wafer being configured to enable a partial through-cut of said third wafer in a vicinity of said recessed portion of said third wafer such that said second component is not damaged during formation of the partial through-cut of said third wafer.

15. The wafer stack of claim 12, wherein said second wafer has a second component, and wherein said third wafer comprises means for enabling a partial through-cut of said third wafer.

16. The wafer stack of claim 13, wherein said first component is configured to enable electrical communication of said first die assembly with a component external to said first die assembly.

17. The wafer stack of claim 15, wherein said means for enabling a partial through-cut comprises means for preventing damage of said second component.

18. A wafer stack defining a plurality of die assemblies, said wafer stack comprising:

a first wafer including a first component; and

a second wafer arranged in an overlying relationship with said first wafer, said second wafer being bonded to said first wafer, said first component being arranged adjacent to said second wafer;

said first wafer and said second wafer defining a gap therebetween, said gap being arranged in an overlying relationship with said first component, said gap being configured to enable a partial through-cut of said second wafer in a vicinity of said gap such that said first component is not damaged during formation of the partial through-cut;

wherein a first die assembly of the plurality of die assemblies is defined by at least a portion of said first wafer and at least a portion of said second wafer.

19. The wafer stack of claim 18, wherein said gap is at least partially defined by a recessed portion of said second wafer.

20. The wafer stack of claim 18, further comprising:

a third wafer, said second wafer being arranged at least partially between said first wafer and said third wafer; and

wherein said second wafer has a second component, said third wafer defining a recessed portion arranged in an overlying relationship with said second component, said recessed portion of said third wafer being configured to enable a partial through-cut of said third wafer in a vicinity of said recessed portion of said third wafer such that said second component is not damaged during formation of the partial through-cut of said third wafer.